Logic Families presented by Dr. Ramesh Manza M.Sc., Ph.D., SET, NET, FIETE, IAEng, CSTA, IACSIT, ISSS, Senior Member IEEE, ISCA, IUPRAI Associate Professor, **Bio-Medical Image Processing Laboratory** Department of Computer Science and Information Technology, Dr. Babasaheb Ambedkar Marathwada University, Aurangabad. 431004(MS) India

## **Logic Families**

- Semiconductor devices can be fabricated using two technologies –
- a) Bipolar Technology
- b) Unipolar Technology (or MOS Technology)

Bipolar technology again classified into two types –

- a) Saturated
- b) Unsaturated

#### Classification of Logic Family



## Logic Families

- a) Bipolar Technology :-
- ✓ Uses diodes (transistor) and BJT for fabricating circuits.
- ✓ Fast in operation.
- ✓ Consume lot of power.
- ✔ Good switching speed.
- **b)** Unipolar Technology ( or MOS Technology ) :-
- ✓ Uses FETs (Field Effect Transistors) or MOSFETS (Metal Oxide Semiconductor FET) for circuit fabrication.
- ✓ Slow in operation.
- ✓ Less power required.
- ✓ Better packing density.
- ✓ Eg. :- PMOS, NMOS, CMOS

## Logic Families

#### a) Saturated :-

- ✓ Transistors are driven into saturation (full conduction).
- ✓ Thus, transistors take some time to switch from saturation ( full conduction ) to cut off ( no conduction ).
- ✓ Eg. :- TTL, I2L, HTL, RTL, DTL

#### **b)** Unsaturated :-

- Transistors switches between conduction and no conduction .
- ✓ Faster because the transistors are never driven into full conduction or full non-conduction.
- ✓ Eg. :- ECL, Schottky TTL

## Full Forms – Logic Families

- FET Field Effect Transistor
- MOSFET Metal Oxide Semiconductor FET
- TTL Transistor Transistor Logic
- I2L Integrated Injection Logic
- HTL High Threshold Logic
- DTL Diode Transistor Logic
- RTL Resistor Transistor Logic
- ECL Emitter Coupled Logic
- PMOS P Channel Metal Oxide Semiconductor Field Effect Transistor
- NMOS N Channel Metal Oxide Semiconductor Field Effect Transistor CMOS – Complementary ( both P Channel and N Channel ) Metal Oxide Effect Transistor

- 1. Logic levels
- 2. Switching speed
- 3. Propagation delay
- 4. Power dissipation
- 5. Noise margins
- 6. Fan out and Fan in

**1.** Logic levels :- Logic levels refer to the voltages and currents that represent logic 1 or logic 0.

```
For TTL family \Box logic 0 \Box 0 V \Box 0.4 V
logic 1 \Box 2.4 V \Box 5 V
```

```
For MOS family \Box logic 0 \Box 0 V
logic 1 \Box 1 = Supply voltage Vcc
```

CMOS IC can be operated for supply range of 3V to 15 V. TTL IC operated at 5V.

#### 2. Switching speed :-

- ✓ It decides the speed of operation of a gate and hence in general the response of a gate to the given input.
- ✓ The switching speed is specified in terms of propagation delay time.
- ✓ Smaller the propagation delay, faster is the speed of operation of a logic circuit.
- TTL logic family has higher switching speed as compared to MOS logic family.

#### 3. Propagation delay :-

- ✓ Whenever some input is applied to a logic gate, it takes some time for the transistors (BJT or FET) to be respond switch its state and produce a stable output. This time is called, "propatation delay".
- ✓ The propagation delay of gate is the average transition delay time for the signal to propagate from input to output It is measured in nanoseconds.
- ✓ The shorter the propagation delay, faster will be the operation of the device.
- ✓ In general, BJT based circuit have good switching speed and hence is the faster.
- ✓ Between TTL and ECL, circuit based on ECL are the faster as the transistors are never in full saturation or full cut-off. Hence, switching from one condition to other is faster.
- ✓ FET or MOSFET based circuits are slower in switching states.
- ✓ Propagation delay in ECL is smallest. So they have very fast switching speed.

#### 4. Power dissipation :-

- ✓ It is a measure of the amount of power utilize by the gate for its operation.
- ✓ The power dissipation is defined as power needed by the logic circuit.
- ✓ A BJT requires more power for its operation than FET or MOSFET. Hence, TTL based circuits dissipate more power than FET based circuits.
- ✓ TTL consumes lot of power for its operation.
- ✓ MOSFET consumes litter power and have better packaging density.

#### 5. Noise margins :-

✓ A noise refers to unwanted sudden signals.

- ✓ The ability of logic circuit to tolerate noise signals ( it means presence of noise doesn't change the output of logic gate ) is called , its noise immunity.
  - When this information is expressed quantitatively in terms of current or voltage it is called, "noise margin". The quantative measure of noise immunity is called noise margin.
- ✓ Noise margin can be DC or AC noise margin.
- ✓ A noise is generally a AC signal with some amplitude and pulse rate.
- ✓ If pulse width of noise is greater than or equal to propagation delay of logic circuit, then the noise is treated as DC noise.
- ✓ If pulse width of noise is less than propagation delay of logic circuit, the duration of noise is to small for a circuit to respond. This means the circuit can with stand a noise of specific amplitude if it has a pulse width.

#### 6. Fan out and Fan in :-

- ✓ Fan in :- Number of inputs that a logic gate can handle properly without disturbing the output level. .
- $\checkmark$  It is a number of gates that can provide inputs to a driving gate.

- Fan-Out :- Fan-out is a logic gate refers to the maximum number of loads (gates). A gate can drive without affecting the working of the gates.
- ✓ It is the number of gates which can be driven by a driver gate simultaneously by the output without disturbing the output level.

## CMOS - Complementary MOS

- CMOS logic family uses CMOS ( Complementary MOS ) transistor.
- CMOS uses both P channel and N channel MOSFET.
- CMOS or CMOSFET Advantages :-
- ✓ High input impedance
- ✓ Good packaging density.
- ✓ Very low power dissipation.
- ✓ Suitable for operation with batteries.

## ECL – Emitter Couple Logic

- ECL (Emitter Coupled Logic) can also be named as CML(Collector Mode Logic).
- ECL is non saturated digital logic family.
- The output of ECL provides OR and NOR function. Each input is connected to the base of transistor.
- Characteristics :-
- ✓ Propagation delay is very LOW(<1ns)</p>
- ✓ ECL is **fastest** logic family.
- ECL circuit usually operate with –Ve supplies (+Ve terminal is connected to ground).

## RTL – Resistor Transistor Logic

- RTL is the first logic family which is not available in monolithic form.
- The basic circuit of the RTL logic family is the NOR.
- Each input is associated with one resistor and one transistor.
- The collector of the transistor are tied together at the output.
- The voltage levels for the circuit are 0.2v for the low level and from 1 to 3.6v for the high level.

#### TTL - Transistor-Transistor Logic

- It can perform many digital function and have achieved the most popularity.
- TTL IC are given the numerical designation as 5400 and 7400 series.
- The basic circuit of TTL with totem pole output stage is NAND gate.
- TTL uses a multi-miter transistor at the input and is fast saturation logic circuit.
- The output transistor Q3 and Q4 form a totem- pole connection. This extra output stage is known as totem-pole stage because three output components Q3 and Q4 and Diode are stacked on one another.
- Characteristics :-
- ✓ TTL has greater speed than DTL.
- ✓ Less noise immunity.
- ✓ Power dissipation is 10mw.
- ✓ It has fan-in of 6 and fan-out of 10.
- ✓ Propagation time delay is 5-15nsec.

## DTL – Diode Transistor Logic

- DTL was first commercial available IC logic family in 53/73 series.
- The basic circuit in the DTL logic is the NAND gate.
- Each input associated with one diode.
- The diode and resistor form an AND gate.
- The transistor services as a NOR gate.

#### • Characteristics :-

- a) It has fan-out of 8.
- b) It has high noise immunity.
- c) Power dissipation is 12mw.
- d) Propagation delay is average 30ns.
- e) Noise margin is about 0.7V.

# 1. Which of the following logic has the maximum fan out ? a) RTL b) ECL c) NMOS d) CMOS [NET Jun 2005, Q. 8]

[ NET Jun 2006 Q. 8 ]

# 1. Which of the following logic has the maximum fan out ? a) RTL b) ECL c) NMOS d) CMOS [ NET Jun 2005, Q. 8 ] [ NET Jun 2006 Q. 8 ]

Answer :- d) CMOS

#### 2. Which of the following logic is the fastest ?

a) RTLb) ECLc) HTLd) HCL

[ NET Dec. 2006, Q. 10 ]

#### 2. Which of the following logic is the fastest ?

- a) RTL b) ECL c) HTL
- c) HTL
- d) HCL [NET Dec. 2006, Q. 10]

Answer :- b) ECL

**Explanation :-** Transistors used in ECL are in different amplifier configuration in which they never driven into saturation and so storage time is eliminated.

- **3.** Among the logic families DTL, TTL, ECL and CMOS the family with the least power dissipation.
- a) CMOS
- b) DTL
- c) TTL
- d) ECL [NET Dec. 2007, Q. 10]

- **3.** Among the logic families DTL, TTL, ECL and CMOS the family with the least power dissipation.
- a) CMOS
- b) DTL
- c) TTL
- d) ECL [NET Dec. 2007, Q. 10]

Answer :- a) CMOS

- 4. Among the logic families RTL, TTL, ECL and CMOS the fastest family is -
- a) ECL
- b) CMOS
- c) TTL
- d) RTL [NET Jun. 2008, Q. 7]

- 4. Among the logic families RTL, TTL, ECL and CMOS the fastest family is -
- a) ECL
- b) CMOS
- c) TTL
- d) RTL [NET Jun. 2008, Q. 7]

Answer :- a) ECL

- 5. Extremely low power dissipation and low cost per gate can be achieved in
- a) MOS ICS
- b) CMOS ICS
- c) TTL ICS
- d) ECL ICS

[ NET Dec 2008, Q. 4 ]

- 5. Extremely low power dissipation and low cost per gate can be achieved in
- a) MOS ICS
- b) CMOS ICS
- c) TTL ICS
- d) ECL ICS [NET Dec 2008, Q. 4]

Answer :- b) CMOS ICS

- 6. Which of the following logic families is well suited for high-speed operations ?
- a) TTL
- b) ECL
- c) MOS

[ NET Jun 2012, P- II, Q. 36 ]

d) CMOS

- 6. Which of the following logic families is well suited for high-speed operations ?
- a) TTL
- b) ECL
- c) MOS
- **d) CMOS** [NET Jun 2012, P- II, Q. 36]

Answer :- b) ECL

- 7. CMOS circuits consume power
- a) Equal to TTL
- b) Less than TTL
- c) Twice of TTL
- d) Thrice of TTL

- 7. CMOS circuits consume power
- a) Equal to TTL
- b) Less than TTL
- c) Twice of TTL
- d) Thrice of TTL

#### **Answer :- b) Less than TTL**

**Explanation :-** As in CMOS, one device is ON and One is always OFF, so power consumption is low.

#### 8. In ECL the fan-out capability is

- a) High
- b) Low
- c) Zero

d) Sometimes high and sometimes low

#### 8. In ECL the fan-out capability is

- a) High
- b) Low
- c) Zero

d) Sometimes high and sometimes low

Answer :- a) High Explanation :- If the input impedance is high and the output resistance is low; as a result, the transistors change states quickly, gate delays are low, and the fan-out capability is high. Fan-out is the measure of the maximum number of inputs that a single gate output can accept.

- 9. Which among the bipolar logic families is specifically adopted for high speed applications ?
  - a. Diode Transistor Logic (DTL)b. Transistor Transistor Logic (TTL)
  - **c.** Emitter Coupled Logic (ECL)
  - **d.** Integrated Injection Logic (I<sup>2</sup>L)

9. Which among the bipolar logic families is specifically adopted for high speed applications ?

a. Diode Transistor Logic (DTL)
b. Transistor Transistor Logic (TTL)
c. Emitter Coupled Logic (ECL)

**d.** Integrated Injection Logic (I<sup>2</sup>L)

**Answer :- Emitter Coupled Logic (ECL)** 

## 10. Which type of unipolar logic family exhibits its usability for the applications requiring low power consumption? a. PMOS b. NMOS

- c. CMOS
- **d.** All of the above

## 10. Which type of unipolar logic family exhibits its usability for the applications requiring low power consumption?a. PMOSb. NMOS

- c. CMOS
- **d.** All of the above

Answer :- c) CMOS

- 11. Which type of unipolar logic family exhibits its usability for the applications requiring low power consumption?
  a. PMOS
  b. NMOS
  c. CMOS
  - **d.** All of the above

- 11. Which type of unipolar logic family exhibits its usability for the applications requiring low power consumption?
  a. PMOS
  b. NMOS
  c. CMOS
  - **d.** All of the above

Answer :- c) CMOS

#### 12. ECL's major disadvantage is that \_\_\_\_\_

a) It requires more powerb) It's fan-out capability is highc) It creates more noised) It is slow

#### 12. ECL's major disadvantage is that \_

a) It requires more powerb) It's fan-out capability is highc) It creates more noised) It is slow

#### Answer :- a) It requires more power

**Explanation :-** ECL's major disadvantage is that each gate continuously draws current, which means it requires (and dissipates) significantly more power than those of other logic families. But ECL logic gates have clock frequency. Thus, they have a fast operation.

#### 13. The ECL circuits usually operates with

- a) Negative voltage
- b) Positive voltage
- c) Grounded voltage
- d) High Voltage

#### 13. The ECL circuits usually operates with

a) Negative voltage
b) Positive voltage
c) Grounded voltage
d) High Voltage

#### Answer :- a) Negative voltage

**Explanation :-** The ECL circuits usually operate with negative power supplies (positive end of the supply is connected to ground), in comparison to other logic families in which negative end of the supply is grounded. It is done mainly to minimize the influence of the power supply variations on the logic levels as ECL is more sensitive to noise on the VCC and relatively immune to noise on VEE.

#### 14. The ECL behaves as \_\_\_\_\_

a) NOT gateb) NOR gatec) NAND gated) AND gate

#### 14. The ECL behaves as \_\_\_\_\_

a) NOT gateb) NOR gatec) NAND gated) AND gate

Answer :- b) NOR gate Explanation :- The ECL behaves as NOR gate because if any of the input voltages go high as compared to the reference voltage, the output is low and the output is high only when all the input voltages are low.

#### 15. In an ECL the output is taken from

- a) Emitter
- b) Base
- c) Collector
- d) Junction of emitter and base

#### 15. In an ECL the output is taken from

- a) Emitter
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- c) Collector
- d) Junction of emitter and base

#### **Answer :- c) Collector**

**Explanation :-** Though, the emitter and collector of the ECL are coupled together. So, the output will be taken from a collector.

d) CCL

16. Sometimes ECL can also be named as

a) EELb) CELc) CMLd) CCL

Answer :- c) CML

**Explanation :-** ECL (Emitter Coupled Logic) can also be named as CML(Collector Mode Logic).

#### 17. Which logic is the fastest of all the logic families ?

- a) TTL b) ECL
- c) HTL
- d) DTL

#### 17. Which logic is the fastest of all the logic families ?

- a) TTL
- b) ECL
- c) HTL
- d) DTL

#### Answer :- b) ECL

**Explanation** :- ECL is the fastest of all the logic families because of the emitters of many transistors are coupled together which results in the highest transmission rate.

#### **18. The full form of ECL is**

a) Emitter-collector logicb) Emitter-complementary logicc) Emitter-coupled logicd) Emitter-cored logic

#### **18. The full form of ECL is**

a) Emitter-collector logicb) Emitter-complementary logicc) Emitter-coupled logicd) Emitter-cored logic

Answer :- c) Emitter-coupled logic

19. Extremely low power dissipation and low cost per gate can be achieved in
(A) MOS ICS
(B) C MOS ICS
(C) TTL ICS
(D) ECL ICS [NET, Dec. 2008, PAPER II, Q. 4]

19. Extremely low power dissipation and low cost per gate can be achieved in
(A) MOS ICS
(B) C MOS ICS
(C) TTL ICS
(D) ECL ICS [NET, Dec. 2008, PAPER II, Q. 4]

Answer :- (B) CMOS ICS

20. Which of the following logic families is well suited for high-speed operations ?
(A) TTL
(B) ECL
(C) MOS
(D) CMOS

20. Which of the following logic families is well suited for high-speed operations ?
(A) TTL
(B) ECL
(C) MOS
(D) CMOS

#### Answer :- (B) ECL

**Explanation :-** ECL stands for Emitter-Coupled Logic. It is designed for extremely high speed application. It is well suited for large mainframe computer that require high number of operation per second.

#### 21. Match the following IC families with their basic circuits :

- a. TTL 1. NAND
- b. ECL 2. NOR
- c. CMOS 3. Inverter Code : a b c
- (A) 1 2 3 (B) 3 2 1
- (C) 2 3 1
- (D) 2 1 3

#### 21. Match the following IC families with their basic circuits :

- a. TTL 1. NAND
- b. ECL 2. NOR
- c. CMOS 3. Inverter Code : a b c
- (A) 1 2 3
- (B) 3 2 1
- (C) 2 3 1 (D) 2 1 3

Answer :- (A) 1 2 3

**Explanation** :-

TTL :- NAND

ECL :- NOR

CMOS :- Inerveter Code : a b c

## 22. Match the following : from position p1, position p2

- a. TTL 1. High fan out
- b. ECL 2. Low propagation delay
- c. CMOS 3. High power dissipation

Code : a b c (A) 3 2 1 (B) 1 2 3 (C) 1 3 2 (D) 3 1 2

## 22. Match the following : from position p1, position p2 a. TTL b. ECL c. CMOS d. High fan out d. High power dissipation

Code :

a b c

#### Answer :- (A) 3 2 1 **Explanation** :-

TTL :- High power dissipation ECL :- Low propagation delay CMOS :- High fan out

#### • Discussion

