

Classification of Microprocessor

presented by

Dr. Ramesh Manza

M.Sc., Ph.D., SET, NET, FIETE, IAEng, CSTA, IACSIT, ISSS, Senior Member

IEEE, ISCA, IUPRAI

Associate Professor,

Bio-Medical Image Processing Laboratory

Department of Computer Science and Information Technology,

Dr. Babasaheb Ambedkar Marathwada University,

Aurangabad. 431004(MS) India

Classification of Microprocessors

- Classification of microprocessor **based on the architecture** i.e. **Instruction Set** of the microprocessor.
 1. RISC - Reduced Instruction Set Computer
 2. CISC - Complex Instruction Set Computer
 3. EPIC - Explicitly Parallel Instruction Computing

RISC - Reduced Instruction Set Computer

- RISC is a microprocessor architecture that is designed to reduce the execution time by simplifying the instruction set of the computer.
- By using RISC processors each instruction requires only one clock cycle to execute results in uniform execution time.
- RISC chips are simple to design and inexpensive.
- This reduces the efficiency as there are many lines of code, hence more RAM is needed to store the instructions.
- The compiler also has to work more to convert high-level language instructions into machine code.
- It is a type of microprocessor architecture that uses a small set of instructions of uniform length. These are simple instructions which are generally executed in one clock cycle.
- The setback of this design is that the computer has to repeatedly perform simple operations to execute a larger program having a large number of processing operations.
- The main idea behind is to make hardware simpler by using an instruction set composed of a few basic steps for loading, evaluating and storing operations just like a load command will load data, store command will store the data.

RISC - Reduced Instruction Set Computer

- **Characteristic** of RISC –
 - Simpler instruction, hence **simple instruction decoding**.
 - Instruction come under **size of one word**.
 - Instruction take **single clock cycle to** get executed.
 - More number of **general purpose register**.
 - Simple **Addressing Modes**.
 - Less Data types.
 - **Pipeline can be achieved**.
- **Examples :-**
 - a) SPARC
 - b) Power PC: 601, 604, 615, 620
 - c) DEC Alpha: 210642, 211066, 21068, 21164
 - d) MIPS: TS (R10000) RISC Processor
 - e) PA-RISC: HP 7100LC

CISC - Complex Instruction Set Computer

- CISC may be designed to minimize the number of instructions per program and ignoring the number of cycles per instruction. The emphasis is on building complex instructions directly into the hardware.
- These processors offer the users, hundreds of instructions of variable sizes.
- CISC architecture includes a complete set of special purpose circuits that carry out these instructions at a very high speed. These instructions interact with memory by using complex addressing modes.
- CISC processors reduce the program size and hence lesser number of memory cycles are required to execute the programs. This increases the overall speed of execution
- The compiler do very little work to translate a high-level language into assembly level language/machine code because the length of the code is relatively short, so very little RAM is required to store the instructions.
- The main idea is that a single instruction will do all loading, evaluating and storing operations just like a multiplication command will do stuff like loading data, evaluating and storing it, hence it's complex.

CISC - Complex Instruction Set Computer

- **Characteristic of CISC –**

- Complex instruction, hence **complex instruction decoding**.
- Instruction are **larger than one word** size.
- Instruction **may take more than single clock cycle** to get executed.
- **Less number of general purpose register** as **operation** get performed **in memory itself**.
- Complex Addressing Modes.
- **More Data types**.

- **Examples-:**

- a) Intel architecture
- b) IBM 370/168
- c) VAX 11/780
- d) Intel 8048
- e) AMD

EPIC - Explicitly Parallel Instruction Computing

- The **best features of** RISC and CISC processors **are combined** in this architecture.
- It **implements parallel processing** of instructions **rather than using fixed length** instructions.
- The working of EPIC processors are **supported by using a set of complex** instructions which **contain both basic** instructions **as well as** the information of execution **of parallel instructions**.
- It substantially **increases the efficiency** of these processors.
- EPIC **breaks through the sequential nature** of conventional processor architectures **by** allowing the **software to communicate** explicitly to the processor **when operations can be done** in parallel. For this, it **uses tighter coupling between** the compiler and the processor.
- It **enables the compiler to extract** maximum parallelism in the original code and explicitly describe it to the processor. Processors based on **EPIC architecture are simpler** and **more powerful** than traditional CISC or RISC processors.
- These processors are **mainly targeted to next-generation**, 64-bit, high end server and workstation market (not for personal computer market).

RISC	CISC
Focus on software	Focus on hardware
Uses only Hardwired control unit	Uses both hardwired and micro programmed control unit
Transistors are used for more registers	Transistors are used for storing complex Instructions
Fixed sized instructions	Variable sized instructions
Can perform only Register to Register Arithmetic	Can perform REG to REG or REG to MEM or MEM to MEM
Requires more number of registers	Requires less number of registers
Code size is large	Code size is small
A instruction execute in single clock cycle	Instruction take more than one clock cycle
A instruction fit in one word	Instruction are larger than size of one word
Very fewer instructions are present. The number of instructions are generally less than 100.	A large number of instructions are present in the architecture.
Instructions with short execution time.	Some instructions with long execution times.
Simple addressing formats are supported. Only base and displacement addressing is allowed.	Multiple formats are supported for specifying operands. A memory operand specifier can have many different combinations of displacement, base and index registers.
RISC does not supports array.	CISC supports array.
Arithmetic and logical operations only use register operands.	Arithmetic and logical operations can be applied to both memory and register operands.
No condition codes are used.	Condition codes are used.
Registers are being used for procedure arguments and return addresses. Memory references can be avoided by some procedures.	The stack is being used for procedure arguments and return addresses.
More registers required.	Less use of registers.
Easy pipelining	Pipelining is difficult
More RAM required	Minimum RAM required.
More compilation process	Less compilation process.
Simple instructions	Instructions are short and complex.

Questions on Microprocessor Architecture

1. **The CISC stands for _____**
- a) Computer Instruction Set Compliment
 - b) Complete Instruction Set Compliment
 - c) Computer Indexed Set Components
 - d) Complex Instruction set computer

Questions on Microprocessor Architecture

1. **The CISC stands for _____**
- a) Computer Instruction Set Compliment
 - b) Complete Instruction Set Compliment
 - c) Computer Indexed Set Components
 - d) Complex Instruction set computer

Answer :- d) Complex Instruction Set Computer

Explanation :- CISC is a computer architecture where in the **processor performs more complex operations in one step.**

Questions on Microprocessor Architecture

2. The computer architecture aimed at reducing the time of execution of instructions is _____
- a) CISC
 - b) RISC
 - c) ISA
 - d) ANNA

Questions on Microprocessor Architecture

2. The computer architecture aimed at reducing the time of execution of instructions is _____
- a) CISC
 - b) RISC
 - c) ISA
 - d) ANNA

Answer :- RISC

Explanation :- The RISC stands for Reduced Instruction Set Computer.

Questions on Microprocessor Architecture

- 3. The RISC processor has a more complicated design than CISC.**
- a) True
 - b) False

Questions on Microprocessor Architecture

3. **The RISC processor has a more complicated design than CISC.**
- a) True
 - b) False

Answer :- False

Explanation :- The RISC processor design is more simpler than CISC and it consists of fewer transistors.

Questions on Microprocessor Architecture

4. In CISC architecture most of the complex instructions are stored in _____
- a) Register
 - b) Diodes
 - c) CMOS
 - d) Transistors

Questions on Microprocessor Architecture

4. In CISC architecture most of the complex instructions are stored in _____
- a) Register
 - b) Diodes
 - c) CMOS
 - d) Transistors

Answer :- Transistors

Explanation :- In CISC architecture **more emphasis is given on the instruction set** and the **instructions take over a cycle** to complete.

Questions on Microprocessor Architecture

5. Which of the architecture is power efficient ?

- a) CISC
- b) RISC
- c) ISA
- d) IANA

Questions on Microprocessor Architecture

5. Which of the architecture is power efficient ?

- a) CISC
- b) RISC
- c) ISA
- d) IANA

Answer :- RISC

Explanation :- Hence the RISC **architecture is followed in the design of mobile devices.**

Questions on Microprocessor Architecture

6. The disadvantage of CISC design processors is

- a) low burden on compiler developers
- b) wide availability of existing software
- c) complex in nature
- d) none of the above

Questions on Microprocessor Architecture

6. The disadvantage of CISC design processors is

- a) low burden on compiler developers
- b) wide availability of existing software
- c) complex in nature
- d) none of the above

Answer C:- Complex in nature

Questions on Microprocessor Architecture

7. The RISC architecture is preferred to CISC because RISC architecture has

- a) Simplicity
- b) Efficiency
- c) High speed
- d) All of the mentioned

Questions on Microprocessor Architecture

7. The RISC architecture is preferred to CISC because RISC architecture has

- a) Simplicity
- b) Efficiency
- c) High speed
- d) All of the mentioned

Answer :- All of the mentioned

Questions on Microprocessor Architecture

- 8. The feature of hybrid CISC-RISC architecture is**
- a) Consume a lot of power
 - b) Not applicable for mobile applications
 - c) Processed by RISC core
 - d) All of the mentioned

Questions on Microprocessor Architecture

8. The feature of hybrid CISC-RISC architecture is

- a) Consume a lot of power
- b) Not applicable for mobile applications
- c) Processed by RISC core
- d) All of the mentioned

Answer :- All of the mentioned

Questions on Microprocessor Architecture

- 9. In order to implement complex instructions, CISC architectures use**
- a) Macroprogramming
 - b) Hardwire
 - c) Microprogramming
 - d) None of the above

Questions on Microprocessor Architecture

9. In order to implement complex instructions, CISC architectures use

- a) Macroprogramming
- b) Hardwire
- c) Microprogramming
- d) None of the above

Answer :- Microprogramming

Questions on Microprocessor Architecture

10. Which of the following processor has a fixed length of instruction ?

- a) CISC
- b) RISC
- c) EPIC
- d) Multi-core

Questions on Microprocessor Architecture

10. Which of the following processor has a fixed length of instruction ?

- a) CISC
- b) RISC
- c) EPIC
- d) Multi-core

Answer :- RISC

Explanation :- The RISC which stands for **Reduced Instruction set computer** has a **fixed length** of instructions. It has a **small instruction set**. Also has **reduced references to memory** to retrieve operands.

Questions on Microprocessor Architecture

11. The advantage of RISC processors is

- a) Can operate at high clock frequency
- b) Shorter design cycle
- c) Simple and fast
- d) All of the mentioned

Questions on Microprocessor Architecture

11. The advantage of RISC processors is

- a) Can operate at high clock frequency
- b) Shorter design cycle
- c) Simple and fast
- d) All of the mentioned

Answer :- All of the mentioned

Questions on Microprocessor Architecture

12. The architecture that uses a tighter coupling between the compiler and the processor

- a) EPIC
- b) Multi-core
- c) RISC
- d) CISC

Questions on Microprocessor Architecture

12. The architecture that uses a tighter coupling between the compiler and the processor

- a) EPIC
- b) Multi-core
- c) RISC
- d) CISC

Answer :- EPIC

Explanation :- EPIC stands for **Explicitly parallel instruction computing**. It has a tighter coupling between the compiler and the processor. It **enables compiler to extract maximum parallelism** in the original code.

Questions on Microprocessor Architecture

13. Processor which is complex and expensive to produce

- a) RISC
- b) EPIC
- c) CISC
- d) Multi-core

Questions on Microprocessor Architecture

13. Processor which is complex and expensive to produce

- a) RISC
- b) EPIC
- c) CISC
- d) Multi-core

Answer :- CISC

Explanation :- CISC stands for **complex instruction set computer**. It is mostly **used in personal** computers. It has a **large instruction set and** a variable length of instructions.

- Logic Families

Thank You