Addressing Modes

presented by Dr. Ramesh Manza

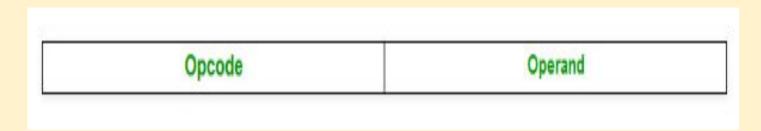
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Addressing Modes

- The term addressing modes refers to the way in which the operand of an instruction is specified.
- The addressing mode specifies a rule for interpreting or modifying the address field of the instruction before the operand is actually executed.
- An assembly language program instruction consists of two parts



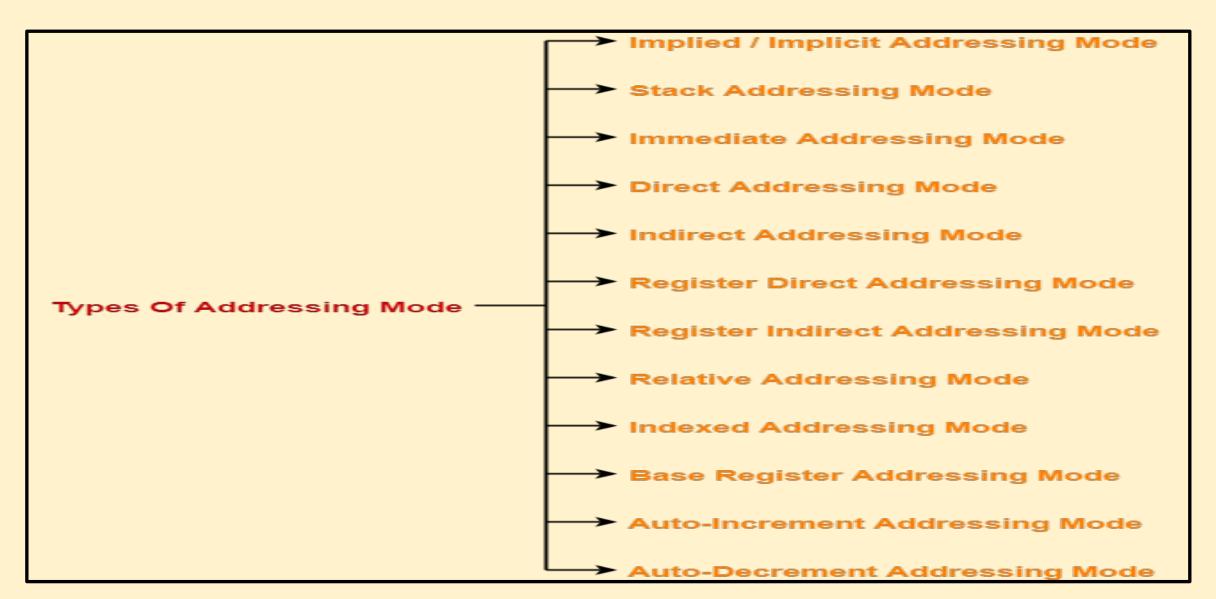
- Operator or opcode \(\square\$ determines what will be done
- Operands □ define the data to be used in the operation

Important Terms

- Starting address of memory segment.
- Effective address or Offset: An offset is determined by adding any combination of three address elements: displacement, base and index.
 - **Displacement:** It is an 8 bit or 16 bit immediate value given in the instruction.
 - Base: Contents of base register, BX or BP.
 - Index: Content of index register SI or DI

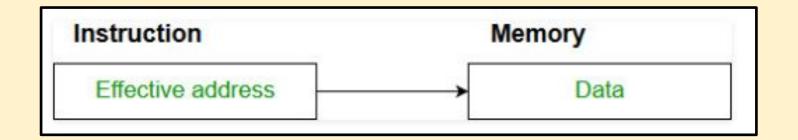
The effective address is a term that describes the address of an operand that is stored in memory. There are several methods to designate the effective address of those operands or get them directly from the register. These methods are known as addressing modes.

Types of Addressing Modes



Direct Addressing Mode / Absolute Addressing Mode

- In this mode, address of the operand is specified in instruction. Here, address of data present in the instruction.
- In this mode the effective address is equal to the address part of the instruction.
- The operand's offset is given in the instruction as an 8 bit or 16 bit displacement element.
- In this addressing mode the 16 bit effective address of the data is the part of the instruction.
- Here only one memory reference operation is required to access the data.
- Eg. :- Add AL, [0301] // Add the contents of offset address 0301 to AL STA 3000 H // Stores accumulator at 16-bit at M. L. 3000 H



Implicit / Implied Addressing Mode

- Instruction that operate only on data in the accumulator are called, "implicit addressing".
- In implied addressing mode, the operand is specified in the instruction itself.
- In this mode, the data is 8 bits or 16 bits long and data is the part of instruction.
- In this, none of the operand is specified. Zero address instruction are designed with implied addressing mode.

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Instruction
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• Eg. :- CLC // Used to reset Carry Flag to 0 HLT // Halt
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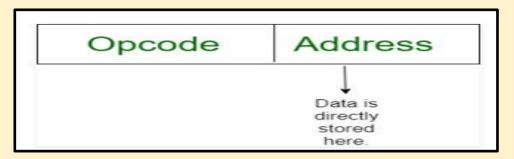
Immediate Addressing Mode

• In this mode the operand is specified in the instruction itself. In other words, an immediate-mode instruction has an operand field rather than an address field. The operand field contains the actual operand to be used in conjunction with the operation specified in the instruction.

• In this mode data is present in address field of instruction .Designed like one address instruction format.

Note: Limitation in the immediate mode is that the range of constants are restricted by size of

address field.



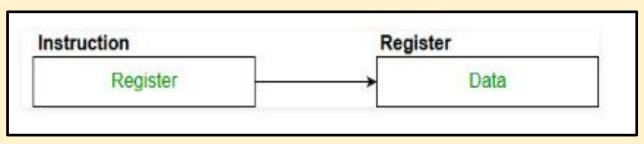
• Eg. :- MOV AL, 35 H □ Move the data 35 H into AL register

ADD 10 □ Increment the value stored in the accumulator by 10

MOV R #20 □ Initializes register R to a constant value 20

Register Addressing Mode

- In this mode, the instruction specifies the register or a register pair. This instruction is of only one byte. Here, all operands are register.
- In this mode, the operands are in registers that reside within in CPU.
- The particular register is selected from a register field in the instruction. A k-bit field can specify any one of 2k registers.
- In register addressing the operand is placed in one of 8 bit or 16 bit general purpose registers. The data is in the register that is specified by the instruction. Here one register reference is required to access the data.



• MOVAX, CX \Box Move the contents of CX register to AX register

Register Indirect Addressing Mode

- In this mode the instruction specifies register in CPU whose contents give the address of the operand in memory.
- Before using a register indirect mode instruction, the programmer must ensure that the memory address of the operand is placed in the processor register with a previous instruction.
- In this addressing the operand's offset is placed in any one of the registers BX,BP,SI,DI as specified in the instruction. The effective address of the data is in the base register or an index register that is specified by the instruction. Here two register reference is required to access the data.



• MOVAX, [BX] \square Move the contents of memory location addressed by the register BX to the register AX

Autoincrement or Autodecrement Mode

- This is similar to the register indirect mode except that the register is incremented or decremented after (or before) its value is used to access memory.
- When the address stored in the register refers to a table of data is memory. It is necessary to increment or decrement the register after every access to the table.

Indirect Addressing Mode

- This addressing mode specifies a register pair which contains memory location address.
- In this mode, the address field of the instruction gives the address where the effective address is stored in memory. Control fetches the instruction from memory and uses its address part to access memory again to read the effective address.

Effective Address = Address part of instruction + content of CPU register

- In this mode address field of instruction contains the address of effective address.
- In this addressing mode, the value of the register serves as another memory location and hence we use pointers to get the data.
- Eg. :- MOV A, M // Move data from mem. Loc. Specified in H-L pair to accumulator

Relative Address Mode

- In this mode the content of the program counter is added to the address part of the instruction in order to obtain the effective address.
- When this number is added to the content of the program counter, the result produces an effective address whose position in memory is relative to the address of the next instruction.

Indexed Addressing Mode

- In this mode the content of an index register is added to the address paid of the instruction to obtain the effective address.
- The operand's offset is the sum of the content of an index register SI or DI and an 8 bit or 16 bit displacement.
- Eg. :- MOV AX, [SI + 05]

Based Indexed Addressing

- The operand's offset is sum of the content of a base register BX or BP and an index register SI or DI.
- Eg. :- ADD AX, [BX + SI]

Base Register Addressing Mode

• In this mode, the content of a base register is added to the address part of the instruction to obtain the effective address.

- 1. In _____ addressing mode, the operands are stored in the memory. The address of the corresponding memory location is given in a register which is specified in the instruction.
 - A) Register direct
 - B) Register indirect
 - C) Base indexed
 - **D)** Displacement

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 - B) Register indirect
 - C) Base indexed
 - **D)** Displacement

Answer :- B) Register indirect

Explanation: In register indirect addressing mode, the operands are stored in the memory. The address of the corresponding memory location is given in a register which is specified in the instruction.

- 2. In _____ addressing mode, the operands are stored in the memory.

 The address of the corresponding memory location is given in a register which is specified in the instruction.
 - A) Register direct
 - B) Register indirect
 - C) Base indexed
 - **D)** Displacement [UGC NET Aug. 2016, P-III, Q. 5]

- 2. In _____ addressing mode, the operands are stored in the memory. The address of the corresponding memory location is given in a register which is specified in the instruction.
 - A) Register direct
 - B) Register indirect
 - C) Base indexed
 - **D)** Displacement

[UGC NET Aug. 2016, P-III, Q. 5]

Answer :- B) Register indirect

Explanation: In register indirect addressing mode, the operands are stored in the memory. The address of the corresponding memory location is given in a register which is specified in the instruction.

- 3. The addressing mode used in an instruction of the form ADD X, Y is
- a) Absolute
- b) Immediate
- c) Indirect
- d) Relative

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Answer :- a) Absolute

Match each of the high level language statements given on the left hand side with the most natural addressing mode from those listed on the right hand side.

```
1. A[1] = B[J]; a. Indirect addressing
2. while [*A++]; b. Indexed addressing
3. int temp = *x; c. Autoincrement

(A) (1, c), (2, b), (3, a)
(B) (1, a), (2, c), (3, b)
(C) (1, b), (2, c), (3, a)
(D) (1, a), (2, b), (3, c)
```

Match each of the high level language statements given on the left hand side with the most natural addressing mode from those listed on the right hand side.

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- (B) (1, a), (2, c), (3, b) (C) (1, b), (2, c), (3, a)
- (D) (1, a), (2, b), (3, c)

Answer: (C)

Explanation:

```
List 1

1) A[1] = B[J]; b) Index addressing
Here indexing is used

2) while [*A++]; c) auto increment
The memory locations are automatically incremented

3) int temp = *x; a) Indirect addressing
Here temp is assigned the value of int type stored at the address contained in X
```

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Match the following:

	Addressing Mode					Location of operand
a.	Immediate i				i.	Registers which are in CPU Register specifies the address of the operand. Specified in the register
b.					ii.	
c.					iii.	
d.	Register Indirect				iv.	Specified implicitly in the definition of instruction
Cod	les:					
	a	b	c	d		
(1)	iv	iii	i	ii		
(2)	iv	i	iii	ii		
(3)	iv	ii	i	iii		
(4)	iv	iii	ii	i		

- (A) (1)
- **(B)** (2)
- (C)(3)
- (D) (4)

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Match the following:

Addressing Mode a. Implied b. Immediate c. Register d. Register Indirect a b c d (1) iv iii i iii (2) iv i iii ii iii (4) iv iii ii ii (4) iv iii ii ii Coation of operand i. Registers which are in CPU Register specifies the address of the operand. Specified in the register iv. Specified implicitly in the definition of instruction Codes:

- (A) (1)
- (B) (2)
- (C)(3)
- **(D)** (4)

Answer: (A)

Explanation:

- In Implied Addressing Mode location of operand specified implicitly in the definition of instruction
- 2. In **Immediate Addressing Mode** location of operand specified in the register.
- 3. In **Register Addressing Mode** location of operand in registers which are in CPU
- 4. In **Register Indirect Addressing Mode** register specifies the address of the operand

6. The addressing mode which makes use of in-direction pointers is

- a) Indirect addressing mode
- b) Index addressing mode
- c) Relative addressing mode
- d) Offset addressing mode

- 6. The addressing mode which makes use of in-direction pointers is
- a) Indirect addressing mode
- b) Index addressing mode
- c) Relative addressing mode
- d) Offset addressing mode

Answer :- a) Indirect addressing mode

Explanation: In this addressing mode, the value of the register serves as another memory location and hence we use pointers to get the data.

- 7. The addressing mode, where you directly specify the operand value
 - is _____
 - a) Immediate
 - b) Direct
 - c) Definite
 - d) Relative

- 7. The addressing mode, where you directly specify the operand value
 - is _____
 - a) Immediate
 - b) Direct
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 - d) Relative

Answer :- a) Immediate

• Classification of Microprocessor

Thank You