Unit - 2 : Computer System Architecture

by

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References

- i) Fundamental of Digital Electronics 3rd Ed. By A. P. Malvino, THM
- ii) Computer System Architecture by Morris Mano, PHI, 3rd edition

Contents

- 1. Interrupts
- 2. Addressing Modes
- 3. Classification of Microprocessor
- 4. Logic Families

Way of discussion

- Theory
- MCQs asked in NET/SET Exams
- Additional few MCQs
  - Interactive
    - Post your answer in chat window

Interrupt

- An interrupt is a signal to the processor emitted by hardware or software which required attention from processor, an interrupt is serviced on the basis of priority and need.

- It is a condition that halts the microprocessor temporarily to work on a different task and then return to its previous task.

- Interrupt is an event or signal that causes a break in the normal executing of a program and request to attention of CPU. This halt allows peripheral devices to access the microprocessor.

- Interrupts have highest priority than other signals.

- While the processor is handling the interrupts, it must inform the device that its request has been recognized so that it stops sending the interrupt request signal. Also, saving the registers so that the interrupted process can be restored in the future.

- Interrupts are used for data transfer between the peripheral devices and the microprocessor.

Interrupt

- **Interrupt Service Routine (ISR)** :- In I/O devices one of the bus control lines is dedicated for this purpose and is called the Interrupt Service Routine (ISR). An interrupt can stop the currently executed program temporarily and branch to an interrupt service routine.

- **Interrupt Lattency** :- The delay between the time an interrupt is received and the start of the execution of the ISR called, " Interrupt Lattency".

- When microprocessor receives interrupt signals, it sends an acknowledgement **(INTA)** to the peripheral which is requesting for its service.

- When microprocessor receives any interrupt signal from peripheral(s) which are requesting its services, it stops its current execution and program control is transferred to a sub-routine by generating **CALL** signal and after executing sub-routine by generating **RET** signal again program control is transferred to main program from where it had stopped.

- The processor if handles more devices as interrupts then it has **multiple interrupt processing ability.**

Registers Used in Interrupt

- **Interrupt Mask Register :-** The register that stores the bits required to mask the interrupts is **Interrupt mask register**.

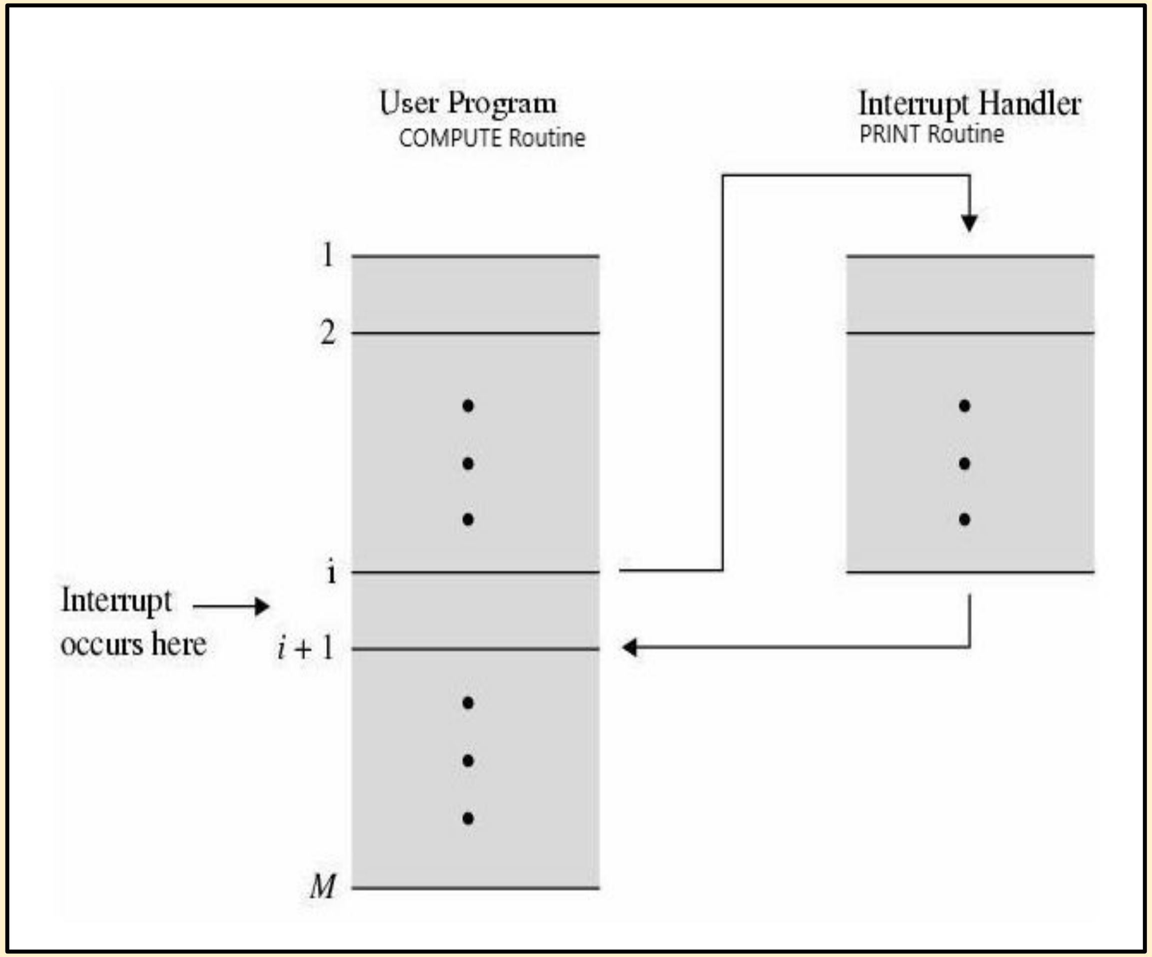
- **Status Register :-** The register that stores the bits required for Status is **Status register.**

- **Interrupt Service Register :-** The register that stores the bits required to service the interrupts is **Interrupt service register.**

- **Interrupt Request Register** :- The register that stores the bits required to request the interrupts is **Interrupt request register**

Interrupt Service Routine (ISR)

The routine that gets executed when an interrupt request is made is called as interrupt service routine.



- Step 1: When the interrupt occurs the processor is currently executing i'th instruction and the program counter will be currently pointing to (i+1)th instruction.
- Step 2: When the interrupt occurs the program counter value is stored on the processes stack.
- Step 3: The program counter is now loaded with the address of interrupt service routine.
- Step 4: Once the interrupt service routine is completed the address on the processes stack is pop and place back in the program counter.
- Step 5: Execution resumes from (i+1)th line of COMPUTE routine.

Classification of Interrupts

1. Hardware Interrupt & Software Interrupt

2. Maskable Interrupt & Non-maskable Interrupt

3. Vectored and Non-vectored Interrupt

Hardware Interrupts (External Interrupt)

- When microprocessors receive interrupt signals through pins (hardware) of microprocessor, they are known as Hardware Interrupts.
- If the signal for the processor is from external device or hardware is called hardware interrupts.
- These are generated by hardware i.e. input-output.
- Eg. :- From keyboard we will press the key to do some action this pressing of key in keyboard will generate a signal which is given to the processor to do action, such interrupts are called hardware interrupts.

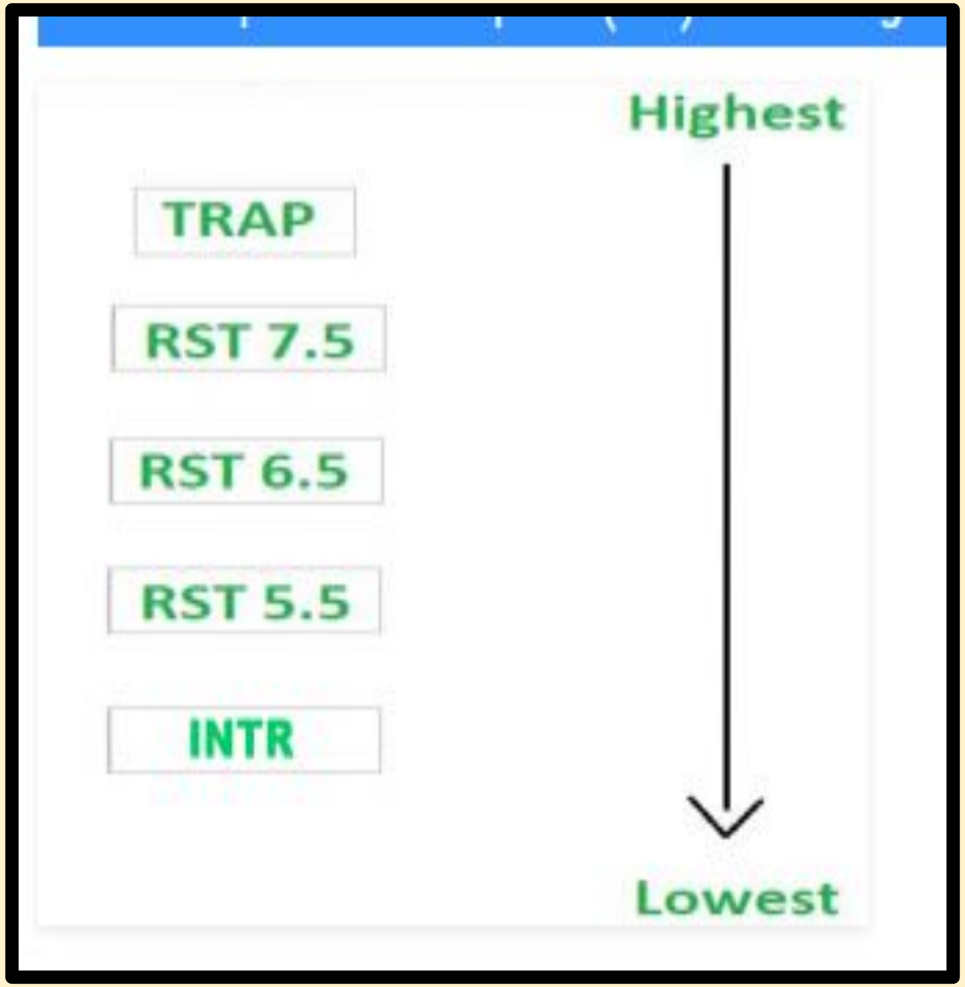
Types of Hardware Interrupts & Priority of Interrupts

- Types of Hardware Interrupts in 8085 microprocessor :- 5

1. TRAP (Highest Priority)
2. RST 7.5
3. RST 6.5
4. RST 5.5
5. INTR (Lowest Priority)

□ INTA (used by microprocessor for sending acknowledgement)

- When microprocessor receives multiple interrupt requests simultaneously, it will execute the interrupt service request (ISR) according to the priority of the interrupts.



Software Interrupts (Internal Interrupt)

- Software Interrupts are those which are inserted in between the program which means these are mnemonics of microprocessor.

- Software interrupts are system calls intentionally written by programmer.

- These are generated by software or instruction or by an exceptional condition.

  These interrupt due to illegal or erroneous use of an instruction or data Eg. :- divide by zero, stack overflow, Invalid opcode, protection violation etc.

- Software Interrupts in 8085 microprocessor :- 8

1. RST 0
2. RST 1
3. RST 2
4. RST 3
5. RST 4
6. RST 5
7. RST 6
8. RST 7

Maskable Interrupts

- Maskable Interrupts are those which can be disabled or ignored or masked by the microprocessor.
- Maskable interrupt can be wait by other instruction when a higher priority interrupt occurs.
- These interrupts are either edge-triggered or level-triggered, so they can be disabled by writing some instruction by software.
- These interrupt can be delayed or rejected or reset by reseting the microprocessor or by DI and SIM instruction.
- Eg. :-

✔ INTR (Level-triggered , maskable and low priority interrupt)

✔ RST 7.5 (Second-highest priority , maskable, edge-triggered interrupt)

✔ RST 6.5 (Third-highest priority, maskable, level-triggered interrupt)

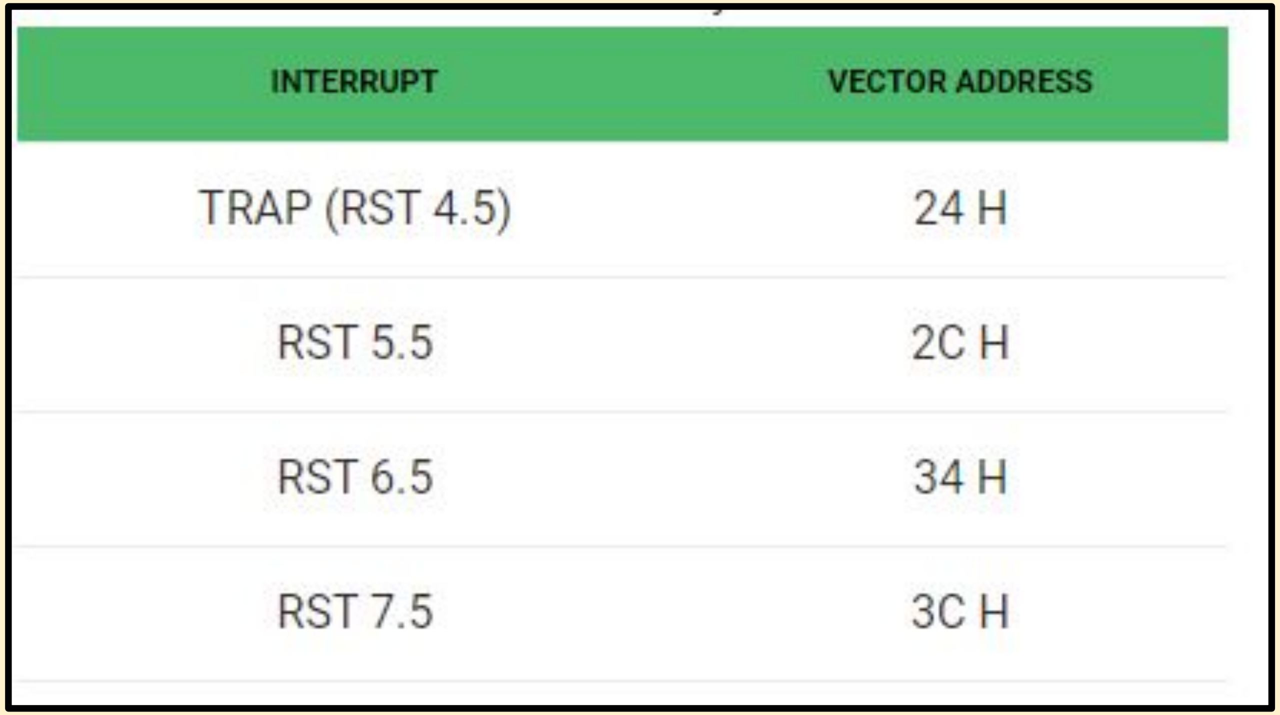
✔ RST 5.5 (Fourht-highest priority, maskable, level-triggered interrupt)

Non-Maskable Interrupts (NMI)

- Non-Maskable Interrupts are those which cannot be disabled or ignored by microprocessor or by other instruction.
- This interrupt can not disabled by sending instruction.
- This interrupt can not be delayed or rejected and should process by the processor immediately.
- It consists of both level-triggering as well as edge-triggering.
- It is used in critical power failure conditions.
- Eg. :- TRAP (Highest priority, non-maskable, edge & level-triggered interrupt)

Vectored Interrupts

- Vectored Interrupts are those which have fixed vector address (starting address of sub-routine) and after executing these, program control is transferred to that address.



INTERRUPT	VECTOR ADDRESS
TRAP (RST 4.5)	24 H
RST 5.5	2C H
RST 6.5	34 H
RST 7.5	3C H

Non-Vectored Interrupts

- Non-Vectored Interrupts are those in which vector address is not predefined.
- The interrupting device gives the address of sub-routine for these interrupts.
- INTR is the only non-vectored interrupt in 8085 microprocessor.
- Vector Addresses are calculated by the formula 8 * TYPE

Interrupt Type	Vector Address in Decimal	Vector Address in Hexadecimal
RST 0	0 * 8 = 0	0000 H
RST 1	1 * 8 = 8	0008 H
RST 2	2 * 8 = 16	0010 H
RST 3	3 * 8 = 24	0018 H
RST 4	4 * 8 = 32	0020 H
RST 5	5 * 8 = 40	0028 H
RST 6	6 * 8 = 48	0030 H
RST 77	7 * 8 = 56	0038 H

Summary of Interrupt

- **Internal Interrupt :-** Interrupt which arises from illegal or erroneous use of an instruction or data. Eg. :- Register overflow, stack overflow, Protection violation.
- **External Interrupt** :- Hardware error like power failure, memory parity error, I/O controller, Timer(internal processor timer is used in pre-emptive multi-tasking)
- **Hardware Interrupt** :- Interrupt generated by hardware. Eg. :- temperature sensor etc.
- **Software Interrupt** :- System calls intentionally written by programmer
- **Asynchronous Interrupt :-** If the interrupts are independent or not in phase to the system clock is called asynchronous interrupt.
- **Periodic Interrupt :-** If the interrupts occurred at fixed interval in timeline then that interrupts are called periodic interrupts.
- **Synchronous Interrupt** :- The interrupt which are dependent on the system clock. Eg. :- Timer service
- **Nested Interrupt** :- If an interrupt occurs while executing a program, and the processor is executing the interrupt, if one more interrupt occurs again, then it is called a nested interrupt.

Questions on Interrupts

1. **The register that stores the bits required to mask the interrupts is ______.**

(A) Status register
(B) Interrupt service register
(C) Interrupt mask register
(D) Interrupt request register [UGC NET CS 2016 , Aug – III , Q. 3]

Questions on Interrupts

1. **The register that stores the bits required to mask the interrupts is ______.**

(A) Status register
(B) Interrupt service register
(C) Interrupt mask register
(D) Interrupt request register [UGC NET CS 2016 , Aug – III , Q. 3]

Answer :- (C)

Explanation :- The register that stores the bits required to mask the interrupts is **Interrupt mask register**.

Questions on Interrupts

2. **Interrupt which arises from illegal or erroneous use of an instruction or data is ---------------**

a) Software interrupt

b) Internal interrupt

c) External interrupt

d) None of the above [UGC NET June 2013, III , Q. 44]

Questions on Interrupts

2. **Interrupt which arises from illegal or erroneous use of an instruction or data is ---------------**

a) Software interrupt

b) Internal interrupt

c) External interrupt

d) None of the above [UGC NET June 2013, III , Q. 44]

Answer :- b) Internal interrupt

Explanation :- An internal interrupt is an interrupt that is caused by a machine instruction processed by the computer processor.

Questions on Interrupts

3. While CPU is executing a program, an interrupt exists then it
----

a) follows the next instruction in the program

b) jumps to instruction in other registers

c) breaks the normal sequence of execution of instructions

d) stops executing the program

Questions on Interrupts

3. While CPU is executing a program, an interrupt exists then it ----------------

a) follows the next instruction in the program
b) jumps to instruction in other registers
c) breaks the normal sequence of execution of instructions
d) stops executing the program

Answer :- c) breaks the normal sequence of execution of instructions

Explanation :- An interrupt function is to break the sequence of operation.

Questions on Interrupts

4. **An interrupt breaks the execution of instructions and diverts its execution to**
   a) Interrupt service routine
   b) Counter word register
   c) Execution unit
   d) control unit

Questions on Interrupts

4. **An interrupt breaks the execution of instructions and diverts its execution to**
   a) Interrupt service routine
   b) Counter word register
   c) Execution unit
   d) control unit

Answer :- a) Interrupt service routine

Explanation :- An interrupt transfers the control to interrupt service routine (ISR). After executing ISR, the control is transferred back again to the main program.

Questions on Interrupts

5. **While executing the main program, if two or more interrupts occur, then the sequence of appearance of interrupts is called ------------**
   a) multi-interrupt
   b) nested interrupt
   c) interrupt within interrupt
   d) nested interrupt and interrupt within interrupt

Questions on Interrupts

5. **While executing the main program, if two or more interrupts occur, then the sequence of appearance of interrupts is called ------------**
   a) multi-interrupt
   b) nested interrupt
   c) interrupt within interrupt
   d) nested interrupt and interrupt within interrupt

Answer :- d) nested interrupt and interrupt within interrupt

Explanation :- If an interrupt occurs while executing a program, and the processor is executing the interrupt, if one more interrupt occurs again, then it is called a nested interrupt.

Questions on Interrupts

6. **Whenever a number of devices interrupt a CPU at a time, and if the processor is able to handle them properly, it is said to have ---------**

   a) interrupt handling ability
   b) interrupt processing ability
   c) multiple interrupt processing ability
   d) multiple interrupt executing ability

Questions on Interrupts

6. **Whenever a number of devices interrupt a CPU at a time, and if the processor is able to handle them properly, it is said to have ---------**

   a) interrupt handling ability
   b) interrupt processing ability
   c) multiple interrupt processing ability
   d) multiple interrupt executing ability

Answer :- d) multiple interrupt processing ability

Explanation :- The processor if handles more devices as interrupts then it has multiple interrupt processing ability.

Questions on Interrupts

7. **NMI stands for**
   a) nonmaskable interrupt
   b) nonmultiple interrupt
   c) nonmovable interrupt
   d) none of the mentioned

Questions on Interrupts

7. **NMI stands for**

   a) nonmaskable interrupt
   b) nonmultiple interrupt
   c) nonmovable interrupt
   d) none of the mentioned

Answer :- a) nonmaskable interrupt

Explanation :- NMI is the acronym for nonmaskable interrupt.

Questions on Interrupts

8. **If any interrupt request given to an input pin cannot be disabled by any means then the input pin is called**

   a) maskable interrupt
   b) nonmaskable interrupt
   c) maskable interrupt and nonmaskable interrupt
   d) none of the mentioned

Questions on Interrupts

8. **If any interrupt request given to an input pin cannot be disabled by any means then the input pin is called**

   a) maskable interrupt
   b) nonmaskable interrupt
   c) maskable interrupt and nonmaskable interrupt
   d) none of the mentioned

Answer :- b) nonmaskable interrupt

Explanation :- A nonmaskable interrupt input pin is one which cannot be masked or disabled by any other instruction.

Questions on Interrupts

9. **The INTR interrupt may be**

a) maskable

b) nonmaskable

c) maskable and nonmaskable

d) none of the mentioned

Questions on Interrupts

9. **The INTR interrupt may be**
a) maskable
b) nonmaskable
c) maskable and nonmaskable
d) none of the mentioned

Answer :- a) maskable

Explanation :- The INTR (interrupt request) is maskable or can be disabled.

Questions on Interrupts

10. **If an interrupt is generated from outside the processor then it is an**

a) internal interrupt
b) external interrupt
c) interrupt
d) none of the mentioned

Questions on Interrupts

10. **If an interrupt is generated from outside the processor then it is an**
    a) internal interrupt
    b) external interrupt
    c) interrupt
    d) none of the mentioned

Answer :- b) external interrupt

Explanation :- If an external device or a signal interrupts the processor from outside then it is an external interrupt.

Questions on Interrupts

11. Which of the following interrupts are unmaskable interrupts ?

a) RST 5.5

b) RST 7.5

c) TRAP

d) Both (a) and (b)

Questions on Interrupts

11. Which of the following interrupts are unmaskable interrupts ?

a) RST 5.5

b) RST 7.5

c) TRAP

d) Both (a) and (b)

Answer :- c) TRAP

Explanation :- TRAP is a highest priority, non-maskable, edge & level-triggered interrupt.

- Addressing Modes

Thank You